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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/696,471	10/29/2003	James A. Ranlett	QN1087.US	6909

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EXAMINER	
CHU, GABRIEL L	
ART UNIT	**PAPER NUMBER**
2114	

DATE MAILED: 10/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/696,471	RANLETT, JAMES A.	
	Examiner	Art Unit	
	Gabriel L. Chu	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1,2 and 4-15* is/are allowed.

6)☒ Claim(s) *3,16 and 18-20* is/are rejected.

7)☒ Claim(s) *17* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 October 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *20050421*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters 1, 2, 3, 4, 6 have been used to designate both elements in digital pot 208 and NVRAM 205. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claim 3 rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.** Referring to claim 3, Applicant claims "the digitally controlled potentiometer is configured as a potentiometer or a variable resistor". It is not clear what Applicant intends by this, as potentiometers are variable resistors. It is further unclear in view of page 8 of Applicant's specification in which Applicant has specified

that a "digital potentiometer" means "digitally controlled potentiometers that include variable resistors and traditional potentiometers".

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. **Claims 16, 19 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5818781 to Estakhri et al. in view of US 5859527 to Cook.** Referring to claim 16, Estakhri discloses a system having a host bus adapter (HBA) coupled to a host system and a memory (Figure 5, elements 22, 25, 24.), comprising:

a resistance component between the HBA and the memory (Figure 7, 88, 90.);

and a voltage divider functionally coupled to the potentiometer (Figure 6, elements 38, 40.).

Although Estakhri does not specifically disclose the resistance component may be a digitally controlled potentiometer (DCP), the use of DCPs in regulating voltage is known in the art. An example of this is shown by Cook, from line 39 of column 5 (with emphasis), "Since the voltage and current supply circuits can be considered independently it is possible to use a different control method for each variable. Some of the possible control mechanisms include a simple potentiometer where a constant level is adequate, preset levels selected by a switching mechanism, an external modulation

source, a **digitally controlled potentiometer** with manual interface, a digitally controlled potentiometer with microprocessor interface, an internal modulation source (for example an oscillator, envelope generator, voltage controlled oscillator or current controlled oscillator), a microprocessor based waveform synthesiser, a microprocessor based envelope synthesiser, internal feedback synthesis, a Bio-feedback mechanism, EEG controlled waveform and/or envelope synthesis or Digital to Analogue converter." A person of ordinary skill in the art at the time of the invention would have been motivated to use a DCP because it is, as indicated from Cook, a well known method of controlling voltage that further allows variation. Further, Estakhri discloses the resistors are assigned values based on appropriateness, from line 55 of column 7, "Based upon the appropriate ratios of resistance values assigned to each of these resistors, the 5V appearing on input voltage 36 is divided to provide 3.3V at node 92." And further, Estakhri discloses (in another embodiment, but applicable to the broader scope of the invention) that the devices may be operable within a range of voltages, from line 5 of column 9, "It should be noted that performance of this alternative embodiment is highly dependent on the operational specification and performance of the Flash EEPROM devices. That is, if these devices are successfully operational at a wide range of input voltage where there is overlap for example from operations voltage of 5V onto 3.3V, this approach may not be optimal."

6. Referring to claim 19, Estakhri in view of Cook discloses the potentiometer includes a wiper (it is a DCP), which is stepped by an input up/down signal from the adapter (In view of Estakhri, all function of the circuitry stems from adapter signals.).

7. **Claim 18 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5818781 to Estakhri et al. and US 5859527 to Cook as applied to claim 16 above, and further in view of "Digitally Controlled Potentiometer (XDCP(TM))" by Xicor (herein Xicor).** Referring to claim 18, Estakhri in view of Cook discloses the potentiometer is driven by signals from the adapter (Estakhri figure 5, element 26, 36.) and is at least transitionally operational upon power up and/or reset (From line 40 of column 6 of Estakhri, "Upon initialization or power-on of the PC system, the PC system's power supply (not shown) is generally in an unstable state, and signals or voltage levels generated by the system are unknown. During this unstable state, the voltage detector shown in FIG. 6 is active and the enable signal 34 is also enabled (or active) and at logic state "1" in the preferred embodiment. The N2 transistor 42 is "on" ensuring that the resistor-divider circuit comprising R1 and R2, 38 and 40, is active. During system power-on, latch 72 is sampling and thereby capturing the state of the input voltage 36 through the P2 transistor 66 and the N1 transistor 68 because enable signal 34 is active or at logic state "1".). Cook, in disclosing a DCP intrinsically discloses its variability which comprises the ability to increment and decrement, even if these are not necessarily modes.

Although Estakhri in view of Cook does not specifically disclose the DCP may have a increment or decrement mode to be in during power up and/or reset, this is very well known in the art. From Xicor, The position of the wiper element is controlled by the CS, U/D, and INC inputs." Clearly, whether the DCP is stepping its resistance, the DCP must have a mode that predicates in which direction the step will occur. A person of

ordinary skill in the art at the time of the invention would have been motivated to have increment and decrement modes because this is a potentiometer.

8. **Claim 20 rejected under 35 U.S.C. 103(a) as being unpatentable over US 5818781 to Estakhri et al. and US 5859527 to Cook as applied to claim 16 above, and further in view of "nonvolatile random-access memory" by IEEE (herein NVRAM).** Referring to claim 20, Estakhri in view of Cook discloses memory (Estakhri, Flash EEPROM).

Although Estakhri in view of Cook does not specifically disclose the memory may be NVRAM, the use of NVRAM as a memory element is well known in the art. An example of this is shown by IEEE, "A semi-permanent type of data storage (memory) that is backed up by batteries to maintain stored data even if system power is lost. Can be both read and changed by the system." A person of ordinary skill in the art at the time of the invention would have been motivated to use NVRAM because of its accessibility and non-volatility.

Allowable Subject Matter

9. Claims 1, 2, 4-15 allowed.

10. The following is an examiner's statement of reasons for allowance: Referring to claims 1, 2, 4, 5, the prior art does not teach or fairly suggest a system for minimizing memory corruption at power up and/or reset, comprising a digitally controlled potentiometer between an adapter and the memory, in the scope and context of claim 1.

11. Referring to claim 6-15, the prior art does not teach or fairly suggest minimizing memory corruption at power up and/or reset, comprising setting a digitally controlled potentiometer to a resistance value such that upon power up and/or reset data cannot be written to the memory, in the scope and context of claims 6, 11.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

12. Claim 17 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

13. Referring to claim 17, the prior art does not teach or fairly suggest in view of the parent claim the voltage divider includes a pull-down resistor that brings down the voltage at one of the plural potentiometer pins, minimizing the chances of memory corruption.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. See notice of references cited.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gabriel L. Chu whose telephone number is (571) 272-

3656. The examiner can normally be reached on weekdays between 8:30 AM and 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Scott Baderman can be reached on (571) 272-3644. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Gabriel L. Chu
Examiner
Art Unit 2114

gc